

**WHAT IS CLAIMED IS:**

1. A thin film transistor array panel for a liquid crystal display, comprising:
  - an insulating substrate including a display area, a peripheral area around a circumference of the display area, and an outer area comprising other than the display area and the peripheral
  - 5 area;
  - a black matrix formed on the display area of the insulating substrate and having an opening of a matrix array corresponding to pixels;
  - red, blue and green color filters formed at the pixels on the insulating substrate;
  - an insulating layer covering the black matrix and the color filters;
  - 10 a gate wire including a gate line and a gate electrode connected to the gate line, and formed on the insulating layer;
  - a gate insulating layer covering the gate wire on the insulating layer;
  - a semiconductor pattern formed on the gate insulating layer;
  - a data wire including a source electrode and a drain electrode that are made of a same
  - 15 layer on the semiconductor pattern and separated from each other, and a data line connected to the source electrode and defining a pixel in a matrix array by crossing the gate line;
  - a passivation layer covering the data wire and having a first contact hole exposing the drain electrode; and
  - a pixel wire including a pixel electrode connected to the drain electrode through the first
  - 20 contact hole.
2. The thin film transistor array panel of claim 2, further comprising an alignment key formed of a same layer as the black matrix or the color filters of the outer area.

3. The thin film transistor array panel of claim 1, further comprising a common wire formed of the same layer as the black matrix and including a common signal line transmitting a common signal to a common electrode opposing the pixel electrode and common pads transmitting the common signal to the common signal line from external circuits and connected to the common signal line.

4. The thin film transistor array panel of claim 1, wherein the gate wire further includes a gate pad that is connected to and receives a signal from an external circuit, and the data wire further includes a data pad that is connected to and receives a signal from an external circuit, and

wherein the gate pad or the data pad are formed with the same layer as the black matrix, the gate wire, or the data wire on the peripheral area.

5. The thin film transistor array panel of claim 4, wherein the pixel wire further comprises a redundant gate pad and a redundant data pad which are made of a same layer as the pixel electrode and are respectively connected to the gate pad and the data pad through second and third contact holes of the gate insulating layer or the passivation layer.

6. The thin film transistor array panel of claim 5, wherein the gate pad and the data pad are formed of a same layer as the black matrix, and the passivation layer and the gate insulating layer have a fourth and a fifth contact hole to connect the gate pad and the data pad to the gate line and the data line, respectively.

7. The thin film transistor array panel of claim 1, wherein edges of the red, green and blue color filters overlap the black matrix.

5 8. The thin film transistor array panel of claim 1, wherein the insulating layer is planar and is made of organic insulating material.

9. The thin film transistor array panel of claim 1, wherein the black matrix, the gate wire, or the data wire have a single-layered structure made of aluminum, aluminum alloy, copper or copper alloy, or multi-layered structure including a conductive material of chromium, 10 molybdenum, molybdenum alloy, chromium nitride or molybdenum nitride.

10. A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising steps of:

15 forming a black matrix on a display area of an insulating substrate including a display area, a peripheral area around the circumference of the display area, and an outer area comprising an area other than the display area and the peripheral area;

forming red, blue and green color filters on the insulating substrate;

forming an insulating layer covering the black matrix and the color filters;

20 forming an alignment key on the outer area.

forming a gate wire including a gate line and a gate electrode connected to the gate line on the insulating layer;

forming a gate insulating layer covering the gate wire;

forming a semiconductor pattern on the gate insulating layer of the gate electrode;  
forming a data wire including a source electrode and a drain electrode, and a data line  
defining a pixel of a matrix array by crossing the gate line; and  
forming a pixel electrode connected to the drain electrode.

5

11. A thin film transistor array panel for a liquid crystal display, comprising:

a data wire including a data line formed on an insulating substrate;

red, blue and green color filters formed at the pixels on the insulating substrate;

an insulating layer covering the data wire and the color filters;

10 a gate wire including a gate line defining the pixel by crossing the data line and a gate  
electrode connected to the gate line, and formed on the insulating layer;

a gate insulating layer covering the gate wire on the insulating layer, and having a first  
contact hole exposing the data line along with the insulating layer;

a semiconductor pattern formed on the gate insulating layer of the gate electrode; and

15 a pixel wire including a source electrode connected to the data line through the first  
contact hole and a drain electrode, which are made of a same layer on the semiconductor pattern  
and separated from each other, and a pixel electrode connected to the drain electrode and formed  
on the pixels.

20 12. The thin film transistor array panel of claim 11, wherein the edges of the red,  
green and blue color filters overlap the edges of the data line.

13. The thin film transistor array panel of claim 11, wherein the insulating layer is made of organic insulating material.

14. The thin film transistor array panel of claim 11, wherein the gate wire further  
5 includes a gate pad that is connected to the gate line and receives a signal from an external circuit, and the data wire further includes a data pad that is connected to the data line and receives a signal from an external circuit,

wherein the gate insulating layer and the insulating layer have a second and a third contact holes respectively exposing the gate pad and the data pad,

10 wherein the pixel wire further comprises a redundant gate pad and a redundant data pad that are made of a same layer as the pixel electrode and are respectively connected to the gate pad and the data pad through the second and third contact holes.

15 15. The thin film transistor array panel of claim 11, further comprising a first redundant gate pad is formed of a same layer as the data line on the insulating substrate,

wherein the gate wire further includes a gate pad that is connected to the gate line and receives a signal from an external circuit, and the data wire further includes a data pad that is connected to the data line and receives a signal from an external circuit, the gate insulating layer and the insulating layer have a second and a third contact holes, and a fourth contact hole  
20 respectively exposing the first redundant gate pad and the data pad, and the gate pad is connected to the first redundant gate pad through the second contact hole, and

wherein the pixel wire further comprises a second redundant gate pad and a redundant data pad that are made of a same layer as the pixel electrode and are respectively connected to the first redundant gate pad and the data pad through the third and fourth contact holes.

5           16.    The thin film transistor array panel of claim 11, further comprising a light blocking layer formed of a same layer as the data line and overlapping the semiconductor pattern or the gate wire.

10           17.    The thin film transistor array panel of claim 11, further comprising a passivation layer covering at least the semiconductor pattern between the source electrode and the drain electrode.

15           18.    The thin film transistor array panel of claim 17, further comprising a spacer formed on the passivation layer.

            19.    The thin film transistor array panel of claim 18, wherein the spacer is made of photosensitive organic insulating material.

20           20.    The thin film transistor array panel of claim 19, wherein the spacer includes black resin.

            21.    The thin film transistor array panel of claim 11, wherein the semiconductor pattern has a double-layered structure.

22. The thin film transistor array panel of claim 21, wherein the semiconductor pattern includes a first amorphous silicon layer and a second amorphous silicon layer having a band gap lower than that of the first amorphous silicon layer and formed on the first amorphous silicon layer.

23. The thin film transistor array panel of claim 11, wherein the gate insulating layer has a double-layered structure including a lower gate insulating layer and an upper gate insulating layer.

24. The thin film transistor array panel of claim 23, wherein the upper and the lower gate insulating layers include organic insulating material, amorphous silicon nitride, or amorphous silicon oxide.

25. A liquid crystal display, comprising:  
a lower insulating panel including a data wire including a data line formed on a first insulating substrate, red, blue and green color filters formed at the pixels on the first insulating substrate, an insulating layer covering the data wire and the color filters, a gate wire formed on the insulating layer and including a gate line defining a pixel by crossing the data line and a gate electrode connected to the gate line, a gate insulating layer covering the gate wire on the insulating layer and having a first contact hole exposing the data line along with the insulating layer, a semiconductor pattern formed on the gate insulating layer of the gate electrode, and a pixel wire including a source electrode connected to the data line through the first contact hole,

and a drain electrode, which are made of a same layer on the semiconductor pattern and separated from each other, and a pixel electrode connected to the drain electrode and formed on the pixels; and

an upper insulating panel including a common electrode thereon that opposes the lower  
5 insulating panel.

26. The liquid crystal display of claim 25, further comprising a spacer covering a semiconductor pattern between the source electrode and the drain electrode, and maintaining an interval between the upper insulating substrate and the lower insulating substrate.

10

27. The liquid crystal display of claim 26, wherein the spacer is made of photosensitive organic insulating material including black resin.

28. A thin film transistor array panel, comprising:  
15 a plurality of pixels defined by gate lines and data lines; and  
a plurality of thin film transistor and pixel electrodes formed at the pixel and electrically connected to the gate lines and the data lines,

wherein a semiconductor layers of the thin film transistors have a double-layered structure including amorphous silicon layers, which have different band gaps.

20

29. The thin film transistor array panel of claim 28, wherein the semiconductor layers include a first amorphous silicon layer and a second amorphous silicon layer formed on the first

amorphous silicon layer, wherein a band gap of the second amorphous silicon layer is lower than that of the first amorphous silicon layer.

30. A thin film transistor array panel, comprising:

5 a plurality of pixels defined by gate lines and data lines; and  
a plurality of thin film transistor and pixel electrodes formed at the pixel and electrically connected to the gate lines and the data lines,

wherein a gate insulating layer that is one element of the thin film transistor have a double-layered structure including a lower insulating layer and an upper insulating layer.

10

31. The thin film transistor array panel of claim 30, wherein the lower insulating layer and the upper insulating layer are made of organic insulating material, amorphous silicon nitride, or amorphous silicon oxide.

15 32. A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising steps of:

forming a data wire including a data line on an insulating substrate;

forming red, blue and green color filters at the pixels on the insulating substrate;

forming an insulating layer covering the data wire and the color filters;

20 forming a gate wire including a gate line and a gate electrode on the insulating layer;

forming a gate insulating layer covering the gate wire on the insulating layer;

forming a semiconductor pattern and a first contact hole exposing the data line at the insulating layer and the gate insulating layer;

forming ohmic contact layers on the semiconductor pattern; and

forming a pixel wire including a source electrode and a drain electrode on the ohmic contact layers, which are made of a same layer on the semiconductor pattern and separated from each other, and a pixel electrode connected to the drain electrode and formed on the pixels.

5

33. The method of claim 32, wherein the semiconductor pattern has a double-layered structure.

34. The thin film transistor array panel of claim 32, wherein the gate insulating layer  
10 has a double-layered structure including a lower gate insulating layer and an upper gate insulating layer.

35. A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising steps of:

15 forming a data wire including a data line on an insulating substrate;  
forming red, blue and green color filters at the pixels on the insulating substrate;  
forming an insulating layer covering the data wire and the color filters;  
forming a first contact hole and exposing the data line by patterning the insulating layer;  
forming a gate wire including a gate line and a gate electrode connected to the gate line  
20 on the insulating layer;  
forming a gate insulating layer covering the gate wire on the insulating layer;  
forming a semiconductor pattern and exposing the data line through the first contact hole;  
forming ohmic contact layers on the semiconductor pattern; and

forming a pixel wire including a source electrode and a drain electrode on the ohmic contact layers, which are made of a same layer on the ohmic contact layers and separated from each other, and a pixel electrode connected to the drain electrode and formed on the pixels.